Multi-Dimensional Integrated Circuit Connection Network Using LDT

BACKGROUND OF THE INVENTION

TECHNICAL FIELD

The invention relates to computer networks. More particularly, the invention relates to a multi-dimensional integrated circuit connection network that uses an LDT interface.

DESCRIPTION OF THE PRIOR ART

LDT (Lightning Data Transport, also known as HyperTransport) is a point-to-point link for integrated circuits (see, for example, http://www.amd.com/news/prodpr/21042.html). Note: HyperTransport is a trademark of Advanced Micro Devices, Inc. of Santa Clara, California.

HyperTransport provides a universal connection that is designed to reduce the number of buses within the system, provide a high-performance link for embedded applications, and enable highly scalable multiprocessing systems. It was developed to enable the chips inside of PCs, networking, and communications devices to communicate with each other up to 24 times faster than with preexisting standard bus technologies.

Compared with existing system interconnects that provide bandwidth up to 266MB/sec, HyperTransport technology's bandwidth of 6.4GB/sec represents better than a 20-fold increase in data throughput. HyperTransport provides an extremely fast connection that complements externally visible bus standards such as the Peripheral Component Interconnect (PCI), as well as emerging technologies such as InfiniBand. HyperTransport is the connection that is designed to provide the bandwidth that the InfiniBand standard requires to communicate with memory and system components inside of next-generation servers and devices that power the backbone infrastructure of the telecomm industry. HyperTransport technology is targeted primarily at the information technology and telecomm industries, but any application in which high speed, low latency and scalability is necessary can potentially take advantage of HyperTransport technology.

HyperTransport technology also has a daisy-chainable feature, giving the opportunity to connect multiple HyperTransport input/output bridges to a single channel. HyperTransport technology is designed to support up to 32 devices per channel and can mix and match components with different bus widths and speeds.

The Agile engine manufactured by AgileTV of Menlo Park, California (see, also, T. Calderone, M. Foster, *System, Method, and Node of a Multi-Dimensional Plex Communication Network and Node Thereof*, U.S. patent application serial no. 09/679,115 (10/4/00)) uses the LDT technology in a

simple configuration, where an interface/controller chip implements a single LDT connection, and the Agile engine connects one other interface/controller chip (such as the BCM12500 manufactured by Broadcom of Irvine, California) on each node board using LDT. Documented designs also deploy LDT in daisy-chained configurations and switched configurations.

In a daisy-chained configuration (see Figure 1), integrated circuits 10a and 10d communicate over LDT with the cooperation of intermediate integrated circuits 10b and 10c. Each of the intermediate integrated circuits must have two LDT interfaces, and are linked in a one-dimensional, *i.e.* linear, configuration.

In a switched configuration (see Figure 2), a special-purpose integrated circuit 21, *i.e.* an LDT switch, is used to connect multiple integrated circuits 20-20c. Except for the LDT switch, each of the integrated circuits in a switched configuration needs only a single LDT interface.

It would be desirable to provide a system in which a plurality of integrated circuits may be connected using an LDT interface in a multi-dimensional network configuration without requiring an LDT switch.

SUMMARY OF THE INVENTION

The presently preferred embodiment of the invention provides a system in which a plurality of integrated circuits are connected using an LDT interface in a multi-dimensional network configuration without requiring an LDT switch. In

this configuration, each integrated circuit has more than two LDT interfaces. For example, integrated circuits having four LDT interfaces are assembled into a two-dimensional mesh. Integrated circuits having four LDT interfaces can also be linked into a PLEX topology (see T. Calderone, M. Foster, *System, Method, and Node of a Multi-Dimensional Plex Communication Network and Node Thereof*, U.S. patent application serial no. 09/679,115 (10/4/00)). Those skilled in the art will appreciate that integrated circuits with more than two LDT interfaces may form a variety of multi-dimension topologies in addition to the mesh and the PLEX.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block schematic diagram showing a daisy-chained configuration in which a plurality of integrated circuits communicate using an LDT interface with the cooperation of intermediate integrated circuits;

Fig. 2 is a block schematic diagram showing a switched configuration that uses an LDT switch to connect multiple integrated circuits;

Fig. 3 is a block schematic diagram showing a multidimensional configuration using an LDT interface and that does not require an LDT switch according to the invention; and

Fig. 4 is a block schematic diagram showing a PLEX configuration using an LDT interface and that does not require an LDT switch according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

The presently preferred embodiment of the invention (see Figure 3) provides a system in which a plurality of integrated circuits are connected using and LDT interface in a multi-dimensional network configuration without requiring an LDT switch. In this configuration, at least some of the integrated circuits have more than two LDT Interfaces. For example, integrated circuits having four LDT interfaces are assembled into a two-dimensional mesh. Thus, in Figure 3 one integrated circuit 31 has four LDT interfaces, four integrated circuits 32-35 have three LDT interfaces, and four integrated circuits 36-39 have two LDT interfaces. While there are different numbers of LDT interfaces shown in the configuration of Figure 3 with regard to the various integrated circuits, it will be appreciated by those skilled in the art that each of the integrated circuits can have four or more interfaces, where any number of the interfaces, up to the four or more available interfaces, may be used, as required by the architecture in which the integrated circuits are used.

Figure 4 is a block schematic diagram showing a PLEX configuration using an LDT interface that does not require an LDT switch according to the invention (see T. Calderone, M. Foster, *System, Method, and Node of a Multi-Dimensional Plex Communication Network and Node Thereof*, U.S. patent application serial no. 09/679,115 (10/4/00)). For purposes of the discussion herein, PLEX refers to a topology. In Figure 4, each node N1-N16 has two integrated circuits CPU1, CPU2, each of which has three LDT interfaces,

where each of the integrated circuits has a total of four LDT interfaces, the fourth LDT interface coupling the two CPUs together. Figure 4 depicts a two-dimensional NxM PLEX communication grid 600 with N=4 nodes, each node containing six ports, and having two communications processors, as described above. Such topology is a typical PLEX topology. Those skilled in the art will appreciate that the invention herein is readily applicable to other topologies, including both other PLEX topologies and non-PLEX topologies.

Although the invention is described herein with reference to the preferred embodiment, one skilled in the art will readily appreciate that other applications may be substituted for those set forth herein without departing from the spirit and scope of the present invention. Accordingly, the invention should only be limited by the Claims included below.